REMARKS

By this amendment, claims 1-3 have been cancelled, and claims 4-15 have been added. Thus, claims 4-15 are now active in the application. Reexamination and reconsideration of the application is respectfully requested.

The specification and abstract have been carefully reviewed and revised to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the specification and abstract by the current amendment. The attachment is captioned "**Version with markings to show changes made**."

At the top of page 2 of the Office Action, the Examiner required Applicant to submit all publications or documents which are the basis for the drawing figures submitted as prior art in the present application and questioned whether Figs. 3 and 4 show prior art. In this regard, it is noted that only Figs. 5(a) - 6(b) of the present application constitute prior art figures. Figures 3 and 4 show embodiments of the present invention, as described, for example, in the paragraph spanning pages 5 and 6 and in the first paragraph on page 6 of the original specification. Regarding the Examiner's requirement to submit publications or documents on which the prior art drawings were based, copies of JP 2000-091737 and JP 8-340172 were already submitted with an Information Disclosure Statement filed July 28, 2003. An additional reference, JP 6-164119, and its English Abstract, are submitted herewith in a Supplemental Information Disclosure.

Next, in item 1 on page 2 of the Office Action, claims 1-3 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is believed moot in view of the cancellation of claims 1-3. Furthermore, new claims 4-15 have been carefully drafted to avoid the problems enumerated by the Examiner and to otherwise clearly comport with the requirements of 35 U.S.C. 112, second paragraph.

In items 2-5 on pages 3 and 4 of the Office Action, claim 1 was rejected under 35 U.S.C. 102(b) as being clearly anticipated by Darveaux et al. (U.S. 6,201,305); and claims 1-3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Darveaux et al. in view of O'Keefe (U.S. 3,610,811). These rejections are believed moot in view of the cancellation of claims 1-3. Furthermore, these rejections are believed clearly inapplicable to the new claims 4-15, for the following reasons.

With exemplary reference to the drawing Figures 1(a) - 4, new claim 4 sets forth a printed circuit board comprising: a substrate 1 having first and second opposite surfaces, a plurality of terminal holes 2 being formed through the substrate 1 from the first surface to the second surface thereof; a first electrically conductive circuit pattern 6 provided on the first surface of the substrate 1; a second electrically conductive circuit pattern 6 provided on the second surface of the substrate 1; terminal hole conductor layers 5 formed on inner circumferences of the terminal holes 2, respectively, and electrically connecting the first electrically conductive circuit pattern 6 with the second electrically conductive circuit pattern 6; wherein each of the first and second electrically conductive circuit patterns 6 comprises a plurality of composite lands, each of the composite lands including a first land 3 having a center hole 2 aligned with one of the terminal holes 2 of the substrate 1 so as to allow the center hole 2 and the terminal hole 2 to receive a terminal of an electric or electronic part or device, and a plurality of second lands 4 each being contiguous to and extending radially outwardly from the first land 3; and wherein, for each of the composite lands, thermal insulating areas 8 are formed radially outwardly of the first land 3 and circumferentially between adjacent ones of the second lands 4, each of the thermal insulating areas 8 being constituted by an area of the substrate 1 that is devoid of a conductive layer thereon so as to inhibit thermal conduction away from the first and second lands 3, 4.

Thus, according to claim 4, the first and second electrically conductive circuit patterns are provided on the opposing first and second surfaces of the substrate 1, respectively. With the circuit patterns formed on both the first and second surfaces of the substrate 1, thermal energy applied to the composite land 3, 4 during soldering would tend to leak from the composite land

to a greater extent than would occur with a single-sided circuit pattern, due to the fact that the thermal energy of the molten solder lump is conducted from the first land 3 on the side having the solder lump via the conductive layer 5 formed in terminal hole 2 to the first land 3 on the second surface opposite the solder lump. As such, the thermal insulating areas 8 are especially important for the printed circuit board recited in claim 4 having the first electrically conductive circuit pattern provided on the first surface of the substrate, the second electrically conductive circuit pattern provided on the second surface of the substrate, and the terminal hole conductive layers 5 formed on the inner circumferences of the terminal holes 2, respectively, and electrically connecting the circuit pattern on the first surface with the circuit pattern on the second surface.

In contrast, in the Darveaux et al. patent, although a circuit pattern is provided on a first surface of substrate 12 and is constituted by the mounting pad 28 and the metal spokes 32 radiating outwardly therefrom, there is no disclosure or suggestion in the Darveaux et al. patent of providing circuit patterns on both the first and second surfaces of the substrate 12, as required by claim 4. The O'Keefe patent was cited by the Examiner apparently for its teaching of "a narrow resist layer around the mounting pad and the spokes." However, the O'Keefe patent is directed to the provision of specific solder resist patterns (see Figs. 5-7) that provide solder resist on portions of the surface parameter of the hole 3 so as to serve as escape paths or ports to allow gases generated within the hole 30 during the soldering process to escape, in order to avoid the formation of pin holes 36 and gas pockets 38 (see Fig. 3 of O'Keefe). Accordingly, it is submitted that a person of ordinary skill in the art would not have been motived by the O'Keefe reference to modify the Darveaux reference in such a manner as to result in or otherwise render obvious the present invention of claim 4. Therefore, it is respectfully submitted that claim 4, as well as claims 5-8 which depend therefrom, are clearly allowable over the prior art of record.

Next, again with exemplary reference to drawing Figures 1(a) - 4, new independent claim 9 sets forth a printed circuit board comprising a substrate 1 having first and second opposite surfaces, a plurality of terminal holes 2 being formed through the substrate 1 from the first surface to the second surface thereof; an electrically conductive circuit pattern 6 provided on the

first surface of the substrate 1; wherein the electrically conductive circuit pattern 6 comprises a plurality of composite lands, each of the composite lands including a first land 3 having a center hole 2 aligned with one of the terminal holes 2 of the substrate 1 so as to allow the center hole 2 and the terminal hole 2 to receive a terminal of an electric or electronic part or device, and a plurality of second lands 4 each being contiguous to and extending radially outwardly from the first land 3; wherein, for each of the composite lands, thermal insulating areas 8 are formed radially outwardly of the first land 3 and circumferentially between adjacent ones of the second lands 4, each of the thermal insulating areas 8 being constituted by an area of the substrate 1 that is devoid of a conductive layer thereon so as to inhibit thermal conduction away from the first and second lands 3, 4; and wherein, for each of the composite lands, a narrow resist layer 7 (see Figs. 1(a) and 1(b)) is formed so as to be arranged along a border between the composite land 3, 4 and each of the thermal insulating areas 8.

As apparently recognized by the Examiner, the Darveaux patent, while disclosing a printed circuit board having a substrate with a conductive circuit pattern on one surface thereof, clearly does not disclose or suggest the presence of a narrow resist layer formed so as to be arranged along a border between a composite land (constituted by a first land having a center hole, and a plurality of second lands extending radially outwardly from the first land) and each of plural thermal insulating areas formed radially outwardly of the first land and circumferentially between adjacent ones of the second lands.

The Examiner cited the O'Keefe reference for disclosing "a circuit board comprised of a substrate, a conductive via hole (30), a mounting pad (26), conductor patterns (22, 24) and a solder resist pattern." The Examiner stated that, in the O'Keefe patent, "[a] solder resist pattern (14) is formed over the surfaces of the substrate and covers portions of the leads and mounting pad (26). The resist are least tangential to the apertures around each conductive via hole ... The solder resist of the prior art may not be the same configuration as the present invention, but one skill[ed] in the art would choose a pattern of cut out for his own structure because it is a matter of design choice."

However, contrary to the Examiner's assertion, the specific resist patterns disclosed in O'Keefe and the specifically-recited arrangement of the narrow resist layer in the present invention are not merely matters of design choice. The O'Keefe patent discloses specific solder resist patterns in Figs. 5-7 that are explicitly disclosed as being arranged so as to provide solder resist on portions of the surface perimeter of the hole 30 to serve as escape paths or ports to allow gases generated during soldering to escape through the paths or ports (see column 4, lines 51-56). The solder resist patterns of O'Keefe are specifically designed for this specific purpose, and therefore, the O'Keefe patent does not provide a teaching or suggestion which would have motivated a person of ordinary skilled in the art to modify the Darveaux et al. arrangement to provide, for each of the composite lands, a narrow resist layer (e.g. 7 in Figs. 1(a) and 1(b) of the present application) formed so as to be arranged along a border between the composite land 3, 4 and each of the thermal insulating areas 8, as required by claim 9.

Accordingly, since the Darveaux et al. patent and the O'Keefe patent clearly do not suggest the provision of the narrow resist layer formed so as to be arranged along a border between the composite land and each of the thermal insulating areas, as required by present claim 9, it is respectfully submitted that a person having ordinary skilled in the art would not have been motived to modify the Darveaux et al. patent or to make any combination of the references of record in such a manner as to result in or otherwise render obvious the present invention of claim 9. Therefore, it is respectfully submitted that claim 9 is clearly allowable over the prior art of record.

Again, with exemplary reference to the present drawing figures, as with original claim 3, claims 10-15 are directed to a soldering structure, and claim 10 sets forth a soldering structure for electric or electronic parts or devices, comprising: a substrate 1 having first and second opposite surfaces, a plurality of terminal holes 2 being formed through the substrate 1 from the first surface to the second surface thereof; a first electrically conductive circuit pattern 6 provided on the first surface of the substrate 1; a second electrically conductive circuit pattern 6 provided on

the second surface of the substrate 1; terminal hole conductor layers 5 formed on inner circumferences of the terminal holes 2, respectively, and electrically connecting the first electrically conductive circuit pattern 6 with the second electrically conductive circuit pattern 6; wherein each of the first and second electrically conductive circuit patterns 6 comprises a plurality of composite lands, each of the composite lands including a first 3 land having a center hole 2 aligned with one of the terminal holes 2 of the substrate 1 so as to allow the center hole 2 and the terminal hole 2 to receive a terminal of one of the electric or electronic parts or devices, and a plurality of second lands 4 each being contiguous to and extending radially outwardly from the first land 3; wherein, for each of the composite lands, thermal insulating areas 8 are formed radially outwardly of the first land 3 and circumferentially between adjacent ones of the second lands 4, each of the thermal insulating areas 8 being constituted by an area of the substrate that is devoid of a conductive layer thereon so as to inhibit thermal conduction away from the first and second lands 3, 4; and wherein, for at least one of the composite lands, a solder lump 10 is formed on the first land 3 for securing the terminal of the respective electric or electronic part or device, the solder lump 10 having a conical shape with the terminal hole 2 being disposed at a center of the conical shape and with outer ribs 9 protruding radially outwardly from the conical shape.

Claim 13 sets forth the same features as claim 10, except that it does not specify the presence of a second electrically conductive circuit pattern on the second surface of the substrate, nor a terminal hole conductive layer formed in each of the terminal holes.

Thus, with the conical solder lump 10 required by each of claims 10 and 13, which has outer ribs 9 protruding radially outwardly from the conical shape, the solder lump has an increased strength so as to hold the terminal of the electric or electronic part or device in the terminal hole 2 even though the solder lump uses a relatively small amount of solder.

In contrast to the invention of claim 10, the Darveaux patent discloses a solder ball 24, not a conical solder lump having radially outwardly protruding outer ribs, as required by claim

10. The O'Keefe patent also fails to disclose or suggest such a conical solder lump having radially outwardly protruding outer ribs.

Accordingly, since the prior art references of record clearly fails to disclose or suggest the present invention as recited in independent claims 10 and 13, it is believed clear that a person of ordinary skilled in the art would not have been motived to modify the Darveaux patent or to make any combination of the references of record in such a manner as to result in or otherwise render obvious the present invention as recited in either of claims 10 and 13. Therefore, it is respectfully submitted that claims 10 and 13, as well as the claims depending therefrom, are clearly allowable over the prior art of record.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is earnestly solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, it is respectfully requested that the Examiner contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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April 6, 2004